APPENDIX

3. (Amended) A semiconductor device as claimed in claim 1 ~~or 2~~, wherein a stack of layered structures is present.

7. (Amended) A semiconductor device as claimed in claim 1 ~~any one of the preceding claims~~, wherein the via lines are patterned in the form of a grid.

8. (Amended) A method of manufacturing a semiconductor device as claimed in claim 1 ~~any one of the preceding claims~~, comprising the steps of:

(f) forming a metal layer;

(g) forming a dielectric layer;

(h) patterning via lines or via grids in the dielectric layer;

(i) filling the patterned via lines or via grids with a conductive material, such as a metal, and preferably tungsten or copper; and

(j) applying a metal bond pad on top of the dielectric layer and the filled via lines or via grids.

11. (Amended) A method as claimed in claim 8 ~~any one of claims 8 to 10~~, wherein the via lines or lines of metal are applied in the form of a grid.